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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SURYAWANSHI, SURESH	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,076	PLANTE ET AL.	
	Examiner	Art Unit	
	Suresh K Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/25/04 amendments*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 6-7, 11 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Chung-Chih (US Patent no 6,470,456 B1).

4. As per claim 1, Chung-Chih teaches

measuring a prior utilization of the computer while a CPU of the computer is idle [Fig. 2; col. 1, lines 45-62]; and

if the prior utilization crosses a threshold, modifying a parameter associated with the CPU [Fig. 2 and 3; col. 1, lines 45-62].

5. As per claim 2, Chung-Chih teaches that the parameter comprises a clock frequency [col. 1, lines 60-62; operation speed].

6. As per claim 3, Chung-Chih teaches that the parameter comprises a voltage [col. 1, lines 60-62; inherent to the system as to reduce the operation speed].

7. As per claim 4, Chung-Chih teaches storing the prior utilization in a utilization history database [Fig. 3].

8. As per claim 5, Chung-Chih teaches accessing the utilization history database [Fig. 3].

9. As per claim 6, Chung-Chih teaches that the threshold indicates that a performance level allocated with the CPU should be increased [Fig. 3].

10. As per claim 7, Chung-Chih teaches applying a system policy to determine whether to increase the performance level of the CPU [Fig. 3].

11. As per claim 11, Chung-Chih teaches

calculating a prior utilization of the CPU while the CPU in idle [Fig. 2; col. 1, lines 45-62]; and

calculating a utilizable CPU performance level using the prior utilization [Fig. 2 and 3; col. 1, lines 45-62].

12. As per claim 14, Chung-Chih teaches changing the CPU performance level to the utilizable CPU performance level [Fig. 2 and 3; col. 1, lines 45-62].

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 8-10, 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung-Chih (US Patent no 6,470,456 B1).

15. As per claim 8, Chung-Chih discloses the invention substantially. Chung-Chih does not expressly disclose about the system policy that comprises a heat performance limit related to a temperature sensed near the CPU. But Chung-Chih is aware of the temperature reduction in the system by reducing the clock speed of the CPU. However, a routineer would know about a temperature sensor to monitor the temperature of a CPU as the temperature censor is well known in the art. A temperature sensor is typically used in all computers and especially in small size computers such as, laptops, notebooks, palmtops, etc. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system policy or the history database with a heat performance limit related to a temperature sensor near the CPU.

Moreover, a heat performance limit will be advantageous as a system will be prevented from over heating.

16. As per claim 9, Chung-Chih discloses the invention substantially. Chung-Chih does not expressly disclose about the system policy that comprises a battery performance limit related to a battery level of a battery supplying the computer with power. However, a routineer in the art would know that a computer running with a battery usually comprises with a device or circuitry to monitor the level of the battery. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system policy or the history database with a battery performance limit related to a battery level of a battery supplying the computer with power. Moreover, a battery performance limit will be advantageous to indicate a user about the time left for processing and control the CPU speed in such a way to provide a longer time to keep the system running.

17. As per claim 10, Chung-Chih discloses the invention substantially. Chung-Chih does not expressly disclose about the system policy relates to a switching latency of the CPU. However, a routineer in the art would know about a switching latency of a CPU and typically the latency due to performance state transition is limited to no more than approximately two hundred microseconds. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system policy so that it relates to a switching latency of the CPU.

18. As per claim 12, Chung-Chih discloses the invention substantially. Chung-Chih does not expressly disclose about calculating a thermal performance limit. But Chung-Chih is aware of the temperature reduction in the system by reducing the clock speed of the CPU. However, a routineer would know how to calculate a thermal CPU performance limit using the temperature information associated with the CPU as it is well know in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention for changing the CPU performance level to a minimum of the utilizable CPU performance level and the thermal CPU performance limit. Moreover, the thermal CPU performance limit will ensure that the system will operate without getting over heated and so saving a circuitry of the system get damaged.

19. As per claim 13, Chung-Chih discloses the invention substantially. Chung-Chih does not disclose changing the CPU performance level to the battery CPU performance limit if the battery CPU performance limit is the lowest one. However, as explained above in claims 8, 9 and 12, a routineer in the art would be able to combine the all information and build a CPU performance level change accordingly. Therefore, it would have been obvious to one of ordinary skill in the at the time the invention was made to modify the invention so that the battery CPU performance limit will be in effect when it is the lowest one at the time. Moreover, it would be quite obvious that by giving the battery CPU performance limit preference, the system automatically be benefited with both longer battery life and lower heat condition.

20. Claims 15-16, 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung-Chih (US Patent no 6,470,456 B1) in view of Bland et al (US Patent no 5,546,568).

21. As per claim 15, Chung-Chih discloses the invention substantially. Chung-Chih does not disclose about a timer. However, Bland et al expressly disclose a timer that is used to time the idle state of a CPU.[col. 7, lines 49-62]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed towards a method for controlling a CPU clock in response to the CPU being idle. Moreover, it will be advantageous to utilize a timer to ensure that the CPU has been in an idle state for a fixed period of time prior to activating the CPU throttler to account for momentary idle states of the CPU and provide enough time for determining the utilization ratio of the CPU and avoiding mistaken activation of the CPU throttler when the CPU is not idle.

22. As per claim 16, disabling the time if the minimum performance level is equal to a maximum performance level of the CPU [inherent to the system as there is no more performance level for change].

23. As per claim 17, resetting the time if the new performance level is less than a maximum performance level of the CPU [inherent to the system as there is more than one performance level for change].

24. As per claim 18, Chung-Chih teaches

a CPU utilization monitor configured to monitor a utilization of the CPU [Fig. 2; col. 1, lines 45-62; determining a utilization ratio of the CPU];

a CPU throttler configured to perform the adaptive throttling of the CPU based on information from the CPU utilization monitor [Fig. 2 and 3; col. 1, lines 45-65; changing the operation speed according to the CPU utilization ratio].

Chung-Chih does not disclose about a timer to time an idle state of the CPU. But a routineer would know about a timer as it is well known in the art for purpose of timing a CPU state of sleep, idle, power off, and etc. However, Bland et al expressly disclose a timer that is used to time the idle state of a CPU.[col. 7, lines 49-62]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed towards a method for controlling a CPU clock in response to the CPU being idle. Moreover, it will be advantageous to utilize a timer to ensure that the CPU has been in an idle state for a fixed period of time prior to activating the CPU throttler to account for momentary idle states of the CPU and provide enough time for determining the utilization ratio of the CPU and avoiding mistaken activation of the CPU throttler when the CPU is not idle.

25. As per claim 19, Bland et al teach that the CPU is activated when the time since the last idle state exceeds a threshold [col. 7, lines 49-62; predetermined time period].

26. As per claim 20, Chung-Chih and Bland et al disclose the invention substantially. Chung-Chih and Bland et al do not expressly disclose about calculating a thermal policy manager. But they are aware of the temperature reduction in the system by reducing the clock speed of the CPU. However, a routineer would know how to calculate a thermal CPU performance limit using the temperature information associated with the CPU as it is well know in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention for changing the CPU performance level when the temperature crosses a threshold. Moreover, the thermal CPU performance limit will ensure that the system will operate without getting over heated and so saving a circuitry of the system get damaged.

27. As per claim 21, Chung-Chih and Bland et al disclose the invention substantially. Chung-Chih and Bland et al do not expressly disclose about activating the CPU throttler when the charge level of the battery crosses a threshold. However, a routineer in the art would know that a computer running with a battery usually comprises with a device or circuitry to monitor the level of the battery. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system with a battery performance limit related to a battery level of a battery supplying the computer with power. Moreover, a battery performance limit will be advantageous to indicate a user about the time left for processing and control the CPU speed in such a way to provide a longer time to keep the system running.

28. As per claim 22, Chung-Chih teaches that the CPU throttler changes the CPU performance level in response to a utilization of the CPU measured by the CPU utilization monitor [Fig. 2; col. 1, lines 45-62].

29. As per claim 23, Bland et al teach that upon activation, the CPU throttler resets the timer [col. 7, lines 49-62; inherent to the system].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
November 4, 2004